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Carrier, Symbol and Block Synchronizers

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Abstract

The general PLL (Phase Lock Loop) is a device (LOOP) whose VCO (Voltage Controlled Oscillator) is able to follow (LOCK) the input signal phase (PHASE). However, the input signal can be a carrier regular sinusoidal wave, or a symbol/ bit/ data random stream, or a block of bits. So, in this direction, we have respectively the Carrier Synchronizer (CPLL), the Symbol Synchronizer (SPLL) and the Block Synchronizer (BPLL). The carrier synchronizer can be adapted as synthetizer of frequencies with different carriers. The symbol synchronizer recovers the clock of a synchronous system and can operate at different rhythms. The block synchronizer can produce streams of different bit rates. The three synchronizer prototypes can be adapted to different systems. Other objective is to study the output jitter UIRMS (Unit Interval Root Mean Square) versus input SNR (Signal noise ratio).

Keywords: Synchronism; communication systems; digital telecommunications;

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1. Introduction

The PLL (Phase Lock Loop) is a feedback device that controls its VCO (Voltage Controlled Oscilator) so that it follows the input signal phase and frequency [1,2].

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The PLL has four main blocks namely the phase comparator, the amplification factor, the loop filter and the VCO (Fig.1) [3-5].

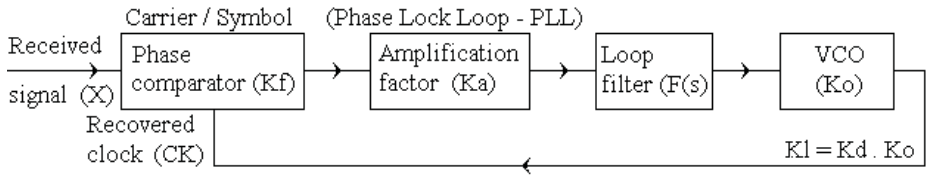

Fig. 1. Blocks diagram of a general PLL

The phase comparator compares the VCO with the input, producing an error pulse that, after amplified and filtered, controls the VCO in order to follow the input [6].

The filter passes the control phase information of low frequency and eliminates the perturbation of high frequency [7-10].

The VCO is a component that provides an output regular wave, whose phase and frequency vary with the input voltage. So, when in synchronism, the VCO frequency is equal to the input carrier frequency (CPLL), or equal to the input stream bit rate (SPLL), or equal to the block frequency conversion ratio fo=(n/m)fi (BPLL) [11].

The amplification factor moves the root locus and consequently the loop desired characteristics [12-15].

The general PLL (CPLL, SPLL, BPLL) has a Lock Range which is the frequency range in which the VCO output, when in lock, is able to follow the input frequency variation. The PLL has also a capture range which is the frequency range in which the VCO, when out of lock, is able to adquire lock with the input. The capture range is normally inferior to the lock range. In practice, some PLL uses a scanning generator in order to increase and become the capture range similar with the lock range.

Following, we present the CPLL whose VCO is able to synchronize with an input carrier regular sinusoidal wave.

Next, we present the SPLL whose VCO is able to synchronize with an input symbol / bit random data stream.

After, we present the BPLL whose VCO is able to synchronize with an input frequency fi related with fo = (n/m)fi.

Next, we show the design and the tests. Then, we show the results. Finally, we present the conclusions.

2. Carrier synchronizer (CPLL)

We studied various types of carrier synchronizers namely the analog, the hybrid, the combinational and the sequential. However, for comparison reference, we selected the sequential prototype (CPLL_seq) [12].

2.1. Carrier synchronizer of sequential type (CPLL_seq)

The carrier synchronizer is a carrier PLL whose VCO output is able to follow (lock) the input signal. Here, the input is a deterministic regular sinusoidal wave. So, the input has positive and negative transitions at all the periods T. Then, the VCO (regular wave) can stabilish phase comparisons with the input in all the periods. So, the carrier phase comparator is normally a simple circuit. The phase comparator produces an error pulse that forces the VCO to lock (follow) the input (Fig.2).

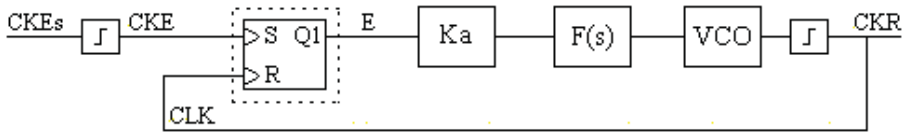

Fig. 2. Carrier Synchronizer of sequential type (CPLL)

The VCO output is a signal (clock) with the same frequency of the input, but with a great quality.

If the input is modulated in frequency, when the VCO output (recovered clock) locks the input signal, then the VCO input is the recovered base band signal that modulated the emitter carrier. The CPLL has a deterministic functionment.

3. Symbol synchronizer (SPLL)

We studied also various types of symbol sysnchronizers namely the analog, the hybrid, the combinational and the sequential. However, for comparison reference, we selected the sequential prototype (SPLL_seq) [13,14].

3.1. Symbol synchronizer of sequential type (SPLL_seq)

The symbol synchronizer is a symbol PLL whose VCO output is able to follow (lock) the input signal. Here, the input is a random symbol data stream. So, the input has positive and negative transitions that can or can not occur (random) in all the periods T (symbol, bit). Then the VCO (regular wave) don't can stabilish phase comparisons with the input in all the periods. So, the symbol phase comparator is normally a more complex circuit. The phase comparator produces an error pulse that forces the VCO to follow (lock) the input (Fig.3)

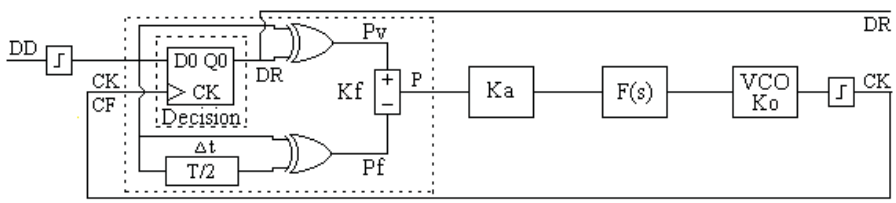

Fig. 3. Symbol Synchronizer of sequential type (SPLL_seq)

The VCO is, normally, a signal clock with a frequency operation equal to the input bit transmisson rate.

The input is a random data symbol sequence and the VCO is the recovered clock that samples and retimes the input. The SPLL has a random functionment.

4. Block synchronizer (BPLL)

We studied various types of block synchronizers namely the analog, the hybrid, the combinational and the sequential. However, for comparison reference, we selected the sequential prototype (BPLL_seq). The block synchronizer can be adapted from the carrier synchronizer working as synthetizer of frequencies [15].

4.1. Block synchronizer of sequential type (BPLL_seq)

The block synchronizer is a block PLL whose VCO output is able to follow (lock) the input signal. Here, the phase comparator inputs are the VCO frequency divided by n and the input frequency divided by m. The phase comparator produces an error pulse that forces the VCO to lock (follow) the input (Fig.4).

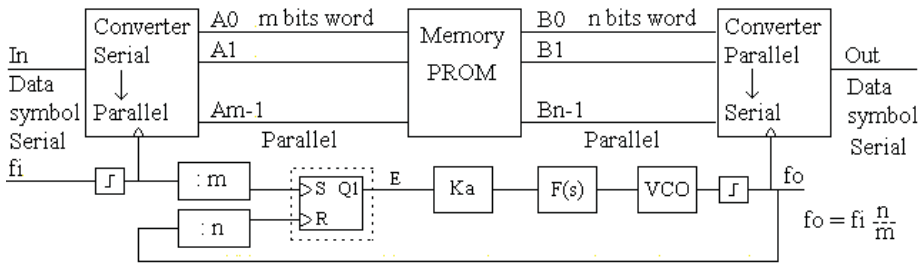

Fig. 4. Block synchronizer of sequential type (BPLL_seq)

The two signal frequencies at the input phase comparator must be equal. Then the input frequency fi divided by m (fi/m) must be equal to the output frequency fo divided by n (fo/n). So, fo/n=fi/m or fo = (n/m)fi.

The block synchronizer is a PLL working as a frequency synthetizer. This BPLL has a deterministic funtionment.

5. Design, tests and results

All the synchronizers have been designed with the same linearized transfer function and they were tested with equal conditions [5].

5.1. Design of the parameters

To compare the various synchronizers in equal conditions, it is necessary to design all the loops with identical linearized transfer functions.

The loop gain is given by Kl=Kd.Ko=Ka.Kf.Ko, where Kf is the phase detector gain, Kd is the phase comparator gain, Ko is the VCO gain and Ka is the control parameter that acts in the root locus providing the desired characteristics.

To test the synchronizer, we used a normalized bit rate tx=1baud, that simplifies the analysis, giving normalized values for the others parameters. So, we used a clock frequency fck=1Hz, an extern noise bandwidth Bn=5Hz and a loop noise bandwidth Bl=0.002Hz. $Ps=A^2_{ef}$ is the signal power and Pn= No.Bn is the noise power. $No =2\sigma n^2.\Delta\tau$ is the noise spectral density and $\Delta\tau=1/fSamp$ is the sampling period.

The relation between SNR and noise variance σn^2 is $SNR = Ps/Pn = A^2_{ef}/(No.Bn) = A^2_{ef}/(2\sigma n^2.\Delta\tau.Bn) = 0.5^2/(2\sigma n^2*10^{-3}*5)= 25/\sigma n^2$.

1-st order loop (the results are similar with the 2-nd order loop)

In the 1-st order loop, the filter F(s) = 0.5Hz eliminates the high frequencies, but mantains the loop characteristics. This cutoff frequency is 25 times greater than Bl=0.02Hz. The transfer function is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (1)$$

and the loop noise bandwidth is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02\text{Hz} \quad (2)$$

So, for the analog synchronizer (Km=1, A=1/2, B=1/2; Ko=2π), the loop bandwidth is

$$Bl=0.02=(Ka.Kf.Ko)/4=(Ka.Km.A.B.Ko)/4=0.02 \rightarrow Ka=0.08*2/\pi \quad (3)$$

For the hybrid synchronizers (Km=1, A=1/2, B=0.45; Ko=2π), the loop bandwidth is

$$Bl=0.02=(Ka.Kf.Ko)/4=(Ka.Km.A.B.Ko)/4=0.02 \rightarrow Ka=0.08*2.2/\pi \quad (4)$$

For the combinational synchronizers (Kf=1/π; Ko=2π), the loop bandwidth is

$$Bl=0.02=(Ka.Kf.Ko)/4=(Ka*1/\pi*2\pi)/4=0.02 \rightarrow Ka=0.04 \quad (5)$$

For the sequential synchronizers (Kf=1/2π; Ko=2π), the loop bandwidth is

$$Bl=0.02=(Ka.Kf.Ko)/4=(Ka*1/2\pi*2\pi)/4=0.02 \rightarrow Ka=0.08 \quad (6)$$

The jitter depends on the signal Aef, noise No and loop noise bandwidth Bl.

For analog PLL the jitter is

$$\sigma\phi^2=Bl.No/Aef^2=Bl.2.\sigma n^2.\Delta\tau=0.02*10^{-3}*2\sigma n^2/0.5^2=16*10^{-5}.\sigma n^2 \quad (7)$$

For the others PLLs the jitter formula is more complicated.

- 2nd order loop:

The second order loop is not analised, but the results are identical to the first order.

5.2. Test setup

To obtain the jitter noise curves of the various synchronizers, we used the following setup (Fig.5) [5].

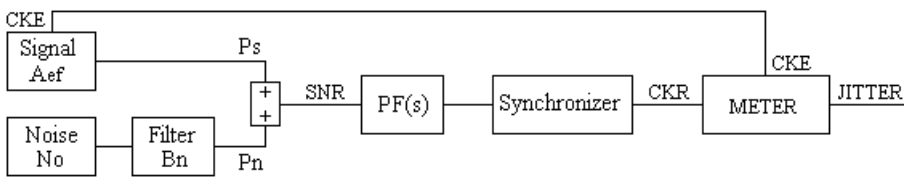

Fig. 5. Blocks diagram of the test setup

The signal noise ratio SNR is given by Ps/Pn, where Ps is the signal power and Pn is the noise power. They are defined as $Ps=Aef^2$ and $Pn= No.Bn = 2\sigma n^2.\Delta\tau.Bn$. Aef is the RMS amplitude, Bn is the extern noise bandwidth, No is the noise power spectral density, σn is the noise standard deviation and Δτ is the sampling period (inverse of samples per time unit). Here, we don't use the prefilter (PF(s)=1).

5.3. Jitter measurer

Fig.6 shows the jitter measurer (M), which consists of a flip flop RS that detects the phase variation of the recovered clock (VCO) relatively to the fixed phase of the emitter clock. This random phase variation is the jitter of the recovered clock [5].

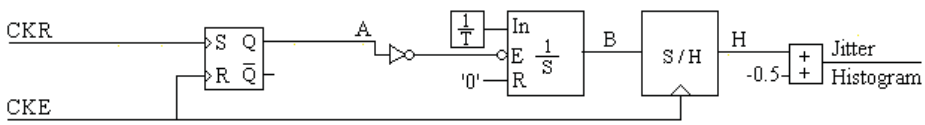

Fig. 6. The jitter measurer

The other blocks convert this phase variation into an amplitude variation which is the jitter histogram.

5.4. Results and discussion

Fig.7 shows the jitter - SNR curves (output jitter UIRMS versus input SNR) of the three prototypes, namely the carrier synchronizer (CPLL), symbol synchronizer (SPLL) and block synchronizer (BPLL).

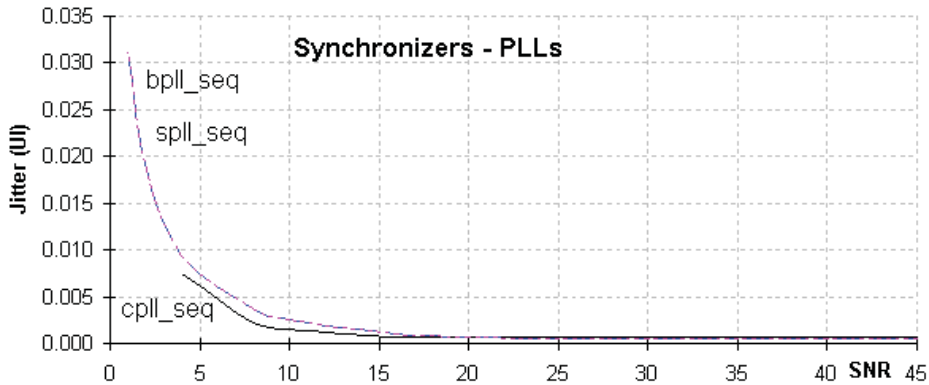

Fig.7. Jitter-SNR curves of the synchronizers CPLL_seq, SPLL_seq and BPLL_seq

We see that, in general, the output jitter decreases gradually with the input SNR increasing.

We verify that, for high SNR, the three synchronizers tend to have similar performance. However, for low SNR, the carrier synchronizer (CPLL) has slightly the better performance.

6. Conclusion and future work

We studied three synchronizer prototypes of sequential type namely the carrier synchronizer (CPLL), the symbol synchronizer (SPLL) and the block synchronizer (BPLL).

We see that, in general for the three prototypes (CPLL, SPLL, BPLL), the output jitter diminishes almost exponentially with the input SNR increasing.

We verify that, for high SNR, the three synchronizers tend to have similar performance. This is compreehensible since the three synchronizers are digital sequential type, with noise margin, and therefore the low noise is ignored.

However, for low SNR in the three synchronizers, the jitter increases significantlly because it depends of the input noise and also of the sequential synchronizer error state caused by noise spikes. In this case, the carrier synchronizer (CPLL) has slightly the better performance. This is compreehensible since it have more transitions per second what corrects more quicly the synchronizer error state.

Acknowledgements

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